AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently amended) A method for fabricating a CCD shift register having silicon electrodes deposited above a substrate~~reading diode of small dimensions between two silicon electrodes deposited above a substrate, said electrodes being a last electrode of a CCD shift register and a reset electrode for emptying electrical charges received by the reading diode from the shift register~~, comprising the following steps:

a) producing ~~the two electrodes~~ a last electrode of the shift register, and a reset electrode, separated by a gap, ~~above the substrate~~;

b) thermally oxidizing a part of a thickness of ~~the~~ said last electrode and said reset electrode~~electrodes~~, in height and in width, leaving a space remaining between the oxidized electrodes, the substrate being protected against oxidation in the space;

c) exposing the surface of the substrate in the space,

d) depositing a layer of doped polycrystalline silicon entering in contact with the substrate in the space in order to form one pole of ~~the~~ a reading diode of small dimensions adapted for converting into a voltage charges conveyed by the shift register, the substrate forming another pole, and said reset electrode being adapted for emptying charges received by said reading diode,

e) partially removing the polycrystalline silicon while leaving a desired pattern remaining, the pattern covering at least the space left between ~~the electrodes~~said last electrode and said reset electrode and also covering a region lying outside the space,

f) depositing an insulating layer, and locally etching an opening into the insulating layer above the polycrystalline silicon outside the space lying between ~~the~~ said last electrode and said reset electrode~~electrodes~~, in order to form an offset contact zone, depositing a metal layer entering in contact with the polycrystalline silicon in the offset contact zone, and etching the metal layer according to a desired pattern of interconnections.

2. (Previously Presented) The method as claimed in claim 1, wherein step e) includes: depositing a uniform layer of silicon nitride and etching according to a pattern which leaves the layer remaining above the polycrystalline silicon zones that are intended to be kept, and the silicon is subsequently oxidized over its entire thickness wherever it is not covered with nitride, until a silicon pattern is obtained which comprises only the zones that were covered with nitride.

3. (Previously Presented) The method as claimed in claim 2, wherein between the deposition of the nitride layer and the subsequent step of oxidizing the polycrystalline silicon, the polycrystalline silicon is chemically attacked in order to remove it as much as possible wherever it is not protected by the nitride.

4. (Currently amended) An integrated circuit comprising:

a CCD register with a readout diode at the end of the register, said readout diode being adapted to convert into a voltage charges conveyed by the shift register and being located between a last electrode of the register and a reset electrode for emptying electrical charges received by the reading diode, wherein the readout diode includes a doped region delimited on one side by the electrodes and on the other side by regions of thick silicon oxide, the doped region being entirely covered with a layer of polycrystalline silicon delimited according to a pattern which extends partly above the thick oxide, the silicon layer being covered with an insulating layer having an opening above the thick oxide but no opening above the doped region, and the insulating layer being itself covered with a conductive layer entering in contact with the polycrystalline silicon through the opening.

5. (Previously Presented) The integrated circuit as claimed in claim 4, wherein the polycrystalline silicon layer is covered with silicon nitride, itself covered by the insulating layer, the nitride layer having the same pattern as the polycrystalline silicon and being open at the position of the opening in the insulating layer.